forming a second pull-up transistor having a third source and a third drain in the second semiconductor structure and a third gate over the second semiconductor structure;

forming a second pull-down transistor having a fourth source and a fourth drain in the substrate, and a fourth gate over the substrate;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact;

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure;

coupling the third source to the fourth contact; and

coupling the third contact to the first voltage input such that the third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

44.(Amended) The method of claim 43, further comprising:

doping the substrate to form a p-type conductivity; and

forming a n-type well within the first semiconductor structure.

45. (Amended) The method of claim 44, further comprising forming a n-type well within the second semiconductor structure.

46. (Amended) A method of fabricating an SRAM memory array comprising:

providing a substrate;

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure within the substrate;

forming a second semiconductor structure within the substrate;

forming a first pull-up transistor having first source and a first drain in the first semiconductor structure and a first gate over the first semiconductor structure;

forming a first pull-down transistor having a second source and a second drain in the substrate and a second gate over the substrate;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor having a third source and a third drain in the second semiconductor structure and a third gate over the second semiconductor structure;

forming a second pull-down transistor having a fourth source and a fourth drain in the substrate and a fourth gate over the substrate;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact;

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure;

coupling the third source to the fourth contact; and

coupling the third contact to the first voltage input such that the third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.

47. (Amended) A method of fabricating a memory device comprising:

forming a first semiconductor structure having a first type region and second type region;

forming a first pull-up transistor having a first source and a first drain in the first type region and a first gate over the first type region;

forming a first pull-down transistor having a second source and a second drain in the second type region and a second gate over the second type region;

forming a first contact and a second contact within the first semiconductor structure;

coupling the first drain to the second drain;

coupling the first gate to the second gate; and

coupling the first source to the second contact; and

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure.

48. (Amended) A method of fabricating a memory device:

forming a first semiconductor structure having a first type region and a second type region and a second semiconductor structure having a first type region and a second type region;

forming a first pull-up transistor within the first semiconductor structure by forming a first source and a first drain in the first type region and a first gate over the first type region;

forming a first pull-down transistor within the first semiconductor structure by forming a second source and a second drain in the second type region and a second gate over the second type region;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source and a third drain in the first type region and a third gate over the first type region;

forming a second pull-down transistor within the second semiconductor structure by forming a fourth source and a fourth drain in the second type region and a fourth gate over the second type region;

forming a third contact and a fourth contact within the second semiconductor structure;

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first source to the second contact;

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure;

coupling the third source to the fourth contact; and

coupling the third contact to the first voltage input such that the third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure.

49. (Amended) The method of claim 48, further comprisingforming a n-type well within the first semiconductor structure.

50. (Amended) A method of fabricating a memory device comprising:

forming a plurality of memory cells arranged in rows and columns, each of the plurality of memory cells fabricated by:

forming a first semiconductor structure having a first type region and a second type region;

forming a second semiconductor structure having a first type region and a second type region;

forming a first pull-up transistor within the first semiconductor structure by forming a first source and a first drain in the first type region and a first gate over the first type region ;

forming a first pull-down transistor within the first semiconductor structure by forming a second source and a second drain in the second type region and a second gate over the second type region ;

forming a first contact and a second contact within the first semiconductor structure;

forming a second pull-up transistor within the second semiconductor structure by forming a third source and a third drain in the first type region and a third gate in the second type region;

forming a second pull-down transistor within the second semiconductor structure by forming a fourth source and a fourth drain in the second type region and a fourth gate over the second type region;

forming a third contact and a fourth contact within the second semiconductor structure;

forming a first terminal and a second terminal of a first access transistor in the substrate;

forming a third terminal and a fourth terminal of a second access transistor in the substrate

coupling the first drain to the second drain and the third drain to the fourth drain;

coupling the first gate to the second gate and the third gate to the fourth gate;

coupling the first terminal to the first and second drains;

coupling the third terminal to the third and fourth drains;

coupling the first source to the second contact;

coupling the first contact to a first voltage input such that the first source is coupled to the first voltage input through parasitic resistance of the first semiconductor structure;

coupling the third source to the fourth contact;

coupling the third contact to the first voltage input such that the third source is coupled to the first voltage input through parasitic resistance of the second semiconductor structure;

coupling the first and second access gates of each of the plurality of memory cells to respective row lines;

coupling the second terminals of each of the plurality of memory cells to respective first column lines; and

coupling the fourth terminals of each of the plurality of memory cells to respective second column lines.